IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney 15761US02

In the Application of:	Bhatia
U.S. Serial No.:	10/600,245
Filed:	6/20/2003
Examiner:	Vo
Group Art Unit:	2621

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This is an appeal from the Office Action made Final mailed March 30, 2009. A Notice of Appeal was filed with the United States Patent and Trademark Office on June 29, 2009.

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I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 5300 California Drive, Irvine California 92617, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-11 and 16-21 are rejected under 35 U.S.C. 103(a) as being obvious from Kono in view of Adolph.

Claims 12-15 are cancelled without prejudice.

The rejection of claims 1-11 and 16-21 under 35 U.S.C. 103(a) are appealed.

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a system (Figure 1, 100)for displaying images on a display. The system comprises:

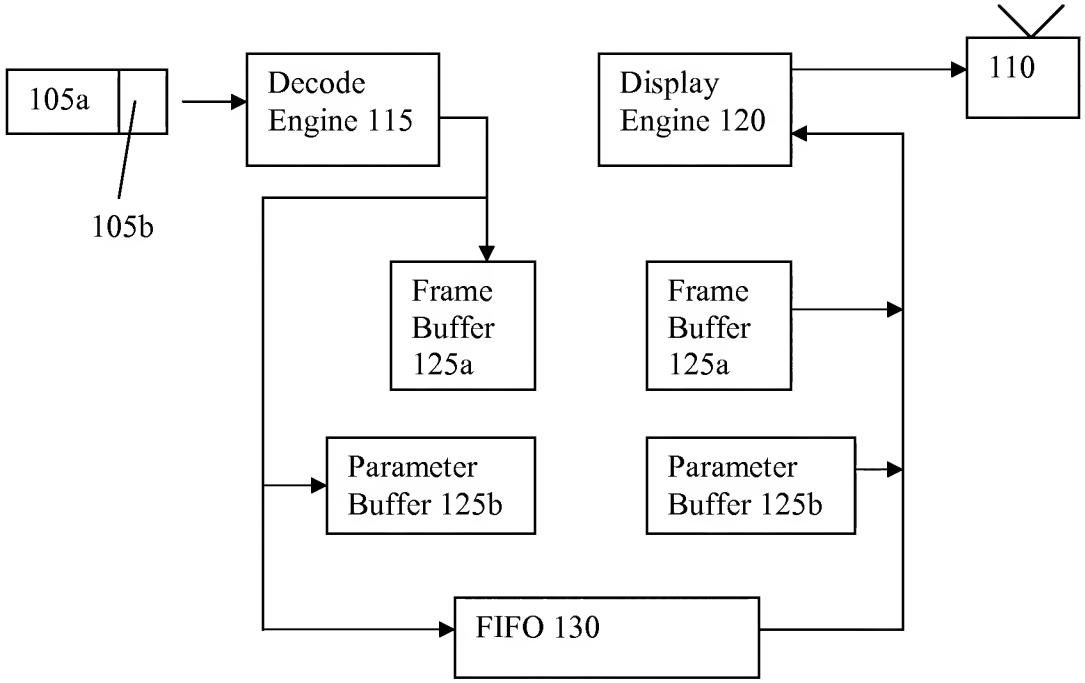
a decoder (Figure 1, decoder engine 115) for decoding encoded images and parameters associated with the images,

thereby resulting in decoded images and decoded parameters associated with the decoded images;

image buffers for storing the decoded images (Frame Buffers 125a, 125b);

a FIFO for storing indicators indicating images to be displayed (FIFO 130); and

a display engine (Figure 1, Display Engine 120) for presenting the images indicated by the FIFO for display.



Specification, FIGURE 1 (Formalized)

Claim 8 is directed to a circuit for displaying images on a display. The circuit comprises:

a processor (CPU 490);

a memory operably coupled to the processor (0054 – "if the processor is available as an ASIC core or logic block, then the commercially available processor can be implemented as part of an ASIC device wherein certain operations are implemented as instruction in firmware),

said memory storing a plurality of executable instructions, wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images (Figure 2, 210);

storing the decoded images (Figure 2, 215);

storing indicators indicating images to be displayed in a FIFO (Figure 2, 222); and

presenting the images indicated by the stored indicators for display (Figure 2, 225, "Retrieve Top Element in FIFO Queue", and "Present image for display using parameters 235").

Claim 11 is directed to a circuit for displaying images on a displa. The circuit comprises:

a first processor (Figure 4, MPEG Video Decoder 445);

a first memory operably coupled to the first processor, said first memory storing a plurality of instructions for execution by the first processor (0054), wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images (Figure 2, 210);

storing the decoded images (Figure 2, 215);

storing indicators indicating images to be displayed in a FIFO (Figure 2, 222); and

a second processor (Figure 4, Display Engine 450) operably coupled to the queue (Figure 4, 475);

a second memory operably coupled to the second processor, said second memory storing a plurality of

instructions for execution by the second processor (0054), wherein the plurality of executable instructions cause:

presenting the images indicated by the indicators for display (Figure 2, 225, "Retrieve Top Element in FIFO Queue", and "Present image for display using parameters 235").

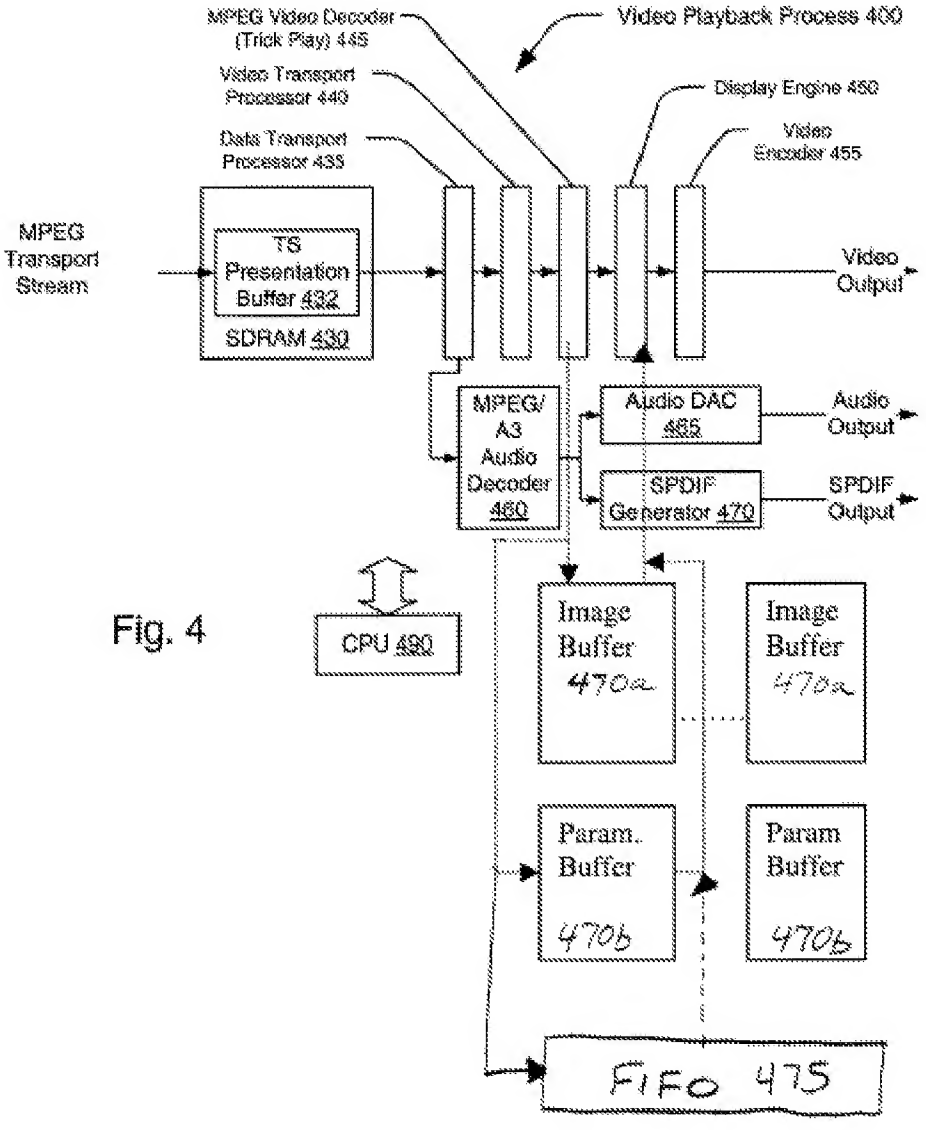


Fig. 4

Specification, FIGURE 4

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 1-11 and 16-21 are obvious under 35 U.S.C. 103(a) from Kono in view of Adolph.

VII. ARGUMENT: CLAIMS 1, 5, 8, 11, AND 16

Claim 1 is copied below:

> A system for displaying images on a display, said system comprising:
>
> a decoder for decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;
>
> image buffers for storing the decoded images;
>
> a FIFO for storing indicators indicating images to be displayed; and
>
> a display engine for presenting the images indicated by the FIFO for display.

Claim 1 was rejected as being obvious from Brailean under 35 U.S.C. 103(a).

A. VIDEO COMPRESSION/DECOMPRESSION

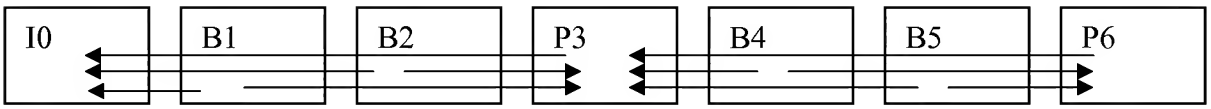
A video camera captures frames from a field of view during time periods known as frame durations. The successive frames form a video sequence. A frame comprises two-dimensional grid(s) of pixels. Common dimensions are, for example, 480 lines by 720 (Standard Definition) or 1080 lines by 1920 (High Definition).

The frames 1…n are encoded using algorithms taking advantage of both spatial redundancy and/or temporal

redundancy. Temporal encoding takes advantage of redundancies between successive frames. A frame can be represented by an offset or a difference frame and/or a displacement with respect to another frame. The encoded frames are known as pictures. Accordingly, video compression standards such as MPEG-2 encode pictures, such that certain pictures are data dependent on other pictures (known as reference pictures).

Exemplary Video Sequence

MPEG-2, for example, defines three types of pictures, I pictures that are not data dependent on other pictures, P pictures that are dependent on one picture that is displayed before it, and B pictures that are dependent on one picture that is displayed before it and one picture that is displayed after it.



An exemplary video includes pictures I0, B1, B2, P3, B4, B5, and P6, where the numerical index indicates the display order. The data dependence of the pictures is illustrated by the arrows. For example, picture B2 is dependent on reference pictures I0 and P3. The foregoing data dependency among the pictures requires decoding of

certain pictures prior to others, such as I0 and P3 before B1 and B2. Additionally, the use of later pictures as reference pictures for previous pictures, requires that the later picture is decoded prior to the previous picture. For example, picture P3 is decoded prior to decoding pictures B1 and B2, and picture P6 is decoded prior to pictures B4 and B5.

The pictures are transmitted in data dependent order, e.g., I0, P3, B1, B2, P6, B4, B5, but displayed as I0, B1, B2, P3, B4, B5, P6. Thus, the pictures will not be displayed in the order that they are received or decoded. Also, after some pictures are decoded, the pictures are not immediately displayed. For example, after picture P3 is decoded and stored, pictures B1 and B2 are decoded and displayed. Then picture P3 is displayed. However, picture P3 remains in storage after P3 is displayed until pictures P6, B4, and B5 are decoded.

Thus, the present invention, e.g., claim 1, includes a decoder for decoding the pictures, an image buffer for storin the pictures, and a display engine for presenting the images for display. Since the decoding order is different from the display order, a FIFO maintains the display order, I0, B1, B2, P3, B4, B5, P6. The display engine uses the FIFO to determine the next picture for display.

B. THE KONO AND ADOLPH REFERENCES

U.S. Pat. Pub. No. 2001/0005398 to Kono is directed to a "Method and a Decoder for Decodin MPEG Video". In Kono, "A decoded picture and parameters of a sequence layer, a GOP layer, and a picture layer respectively for displaying

the decoded picture are stored as a set in each of pictures banks and parameters banks of a frame memory." Kono, however, does not teach the claimed FIFO or that the display engien displays the picture in an order corresponding to the order that the indicators are stored in the FIFO. Office Action (OA) 9/18/08 at 4.

U.S. Patent 6,438,318 to Adolph is directed to a "Method for Regeneratin the Original Data of a Digitally Coded Video Film, and Apparatus for Carrying out the Method". Adolph, Figure 7 is shown below.

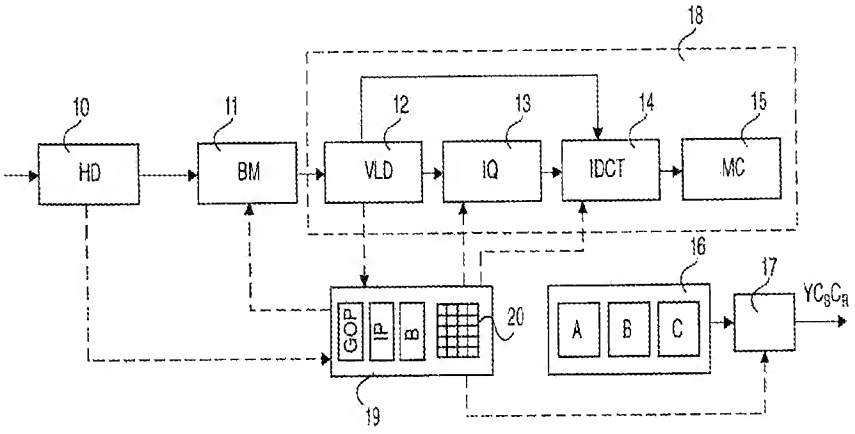


Fig. 7

In Adolph, col. 7, lines 21-40, "The reference number 10 designates a detection circuit for the start codes of the various headers GOP header, picture header, etc. The reference number 11 designates a buffer memory for the read data of the data stream. The reference number 12 designates a decoding unit which reverses the variable length coding of the video data. The reference number 13 designates a processing stage which carries out inverse quantization. The reference number 14 designates a computing circuit in which the DCT transform is reversed. In other words, an

inverse discrete cosine transform takes place. The reference number 15 designates a circuit in which motion compensation for the individual pictures is carried out. Finally, the data decoded in this way are written to the memory unit 16, which contains the three aforementioned frame memories, A, B and C. The reference number 17, finally, designates a post-processing stage."

C. THE REJECTION TO CLAIMS 1, 5, 8, AND 11 SHOULD BE REVERSED BECAUSE THE COMBINATION OF KONO AND ADOLPH DO NOT TEACH "A FIFO FOR STORING INDICATORS INDICATING IMAGES TO BE DISPLAYED" AND "PRESENTING THE IMAGES INDICATED BY THE FIFO FOR DISPLAY."

Claim 1 recites, among other limitations, "a FIFO for storing indicators indicating images to be displayed". Examiner has indicated that "Kono does not particularly teach a queue comprises a FIFO for storing indicators indicating images to be displayed". Previous Office Action, at 3.

However, Examiner has indicated that "Adolph teaches a FIFO (16 of fig. 7) for storing indicators (A,B,C, 16 of fig. 7) indicating images to be displayed, and wherien the queue stores the indicators in a particular order (I, P, B pictures, GOP as display order), and wherein the display engine (fig. 8) displays the picture associated with the indicators (A, B, C) in an order corresponding to the order that the indicators are stored in the queue (20 of fig. fig. 8)." Office Action (OA), 9/18/08 at 5.

Appellant respectfully submits that the foregoin is in error. First, it is noted that memory unit 16 does not even "store indicators". "[M]emory unit 16 … contains the three

aforementioned frame memories, A, B, and C." Adolph, Col. 7, Lines 35-36. It is noted that "A, B, and C" as used in the foregoing, and as would be understood by those skilled in the art are reference labels to individual frame memories in Figure 7. The foregoing would not be understood to mean that memory unit 16 actually stores an "A", a "B", and a "C".

Even if, for the sake of argument, memory unit 16 was held to "store indicators", memory unit 16 is not, and does not perform the same function as a FIFO. A FIFO by definition is a structure that operates on a First In First Out Basis. Adolph does not provide any teaching that memory unit 16 operates on a First In First Out (FIFO) basis.

Appellant calls attention to Kono, Figure 5. "The display order of the pictures is illustrated in the line designated by DIO. The line bearing the reference symbol DEO once again shows the decoding order of the pictures, that is to say the order in which the pictures occur in the bit stream. The line which is designated by the reference symbol FM respectively specifies the frame memory to which the decoded picture located underneath is written."

It can be seen from Figure 5, that B1 is written to frame memory C after P3 is written to frame memory B. However, B1 is displayed and overwritten by B2 before P3 is displayed. Thus, clearly "16 of fig. 7" does not have a First In First Out operation and is not a "FIFO" as claimed. Examiner has also claimed that:

> Adolph teaches that the picture I0 is written into frame memory A after the decoding operation (col. 5, lines 23-24), then picture I0 is released for display (col. 45-47) based upon the command DISP A as indicated (t=t1 of fig. 8), the decoded picture I1 from the memory B is displayed next as indicated DISP B (t=14 of fig.

> 8), and the decoded picture B, from the memory C is display as indicated DISP C (t=t5 of fig. 8). This disclosure fairly suggest the memory (16 of fig. 7) having its indicators (A,B, and C of fig. 7) to indicate the decoded pictures to be displayed (DISP A, DISP b, and DISP c of fig. 8), and the memories A,B, and C store and release the decoded I0, I1, and B pictures for display (the memory A stores I0, col. 5, lines 23-24; the memory B stores I1, col. 5, lines 34-35; the memory C stores B pictures, col. 5, lines 53-54) based on the commands as indicated DISP A, DISP B, and DISP C, this shows that the memory (16 of fig. 7) is a FIFO operation.

Final Office Action, 3/30/09, at 2-3.

The foregoing is in error for several reasons. First, it does not establish that the memory structure 16 stores the indicators A, B, and C. Note that the exemplary commands DISP A, DISP B, DISP C are *not* stored in memory structure 16. Thus, memory structure 16 does not store "a *indicators* indicating images to be displayed". Rather, as note in col. 7, lines 21-40, the memory structure 16 stores the images themselves.

Secondly, although in Figure 4, initially, the frame buffers storing the pictures that are displayed starts with ABC, the order does not continue in that manner:

DEO	BUFFER
I0	A
I1	B
B2	C
P3	A
B4	C
B5	C
B6	C
I7	B

P8 A

I9 B

I10 A

P11 B

P12 A

B13 C

B14 C

P15 B

P16 A

As can be seen, although the first three frames are by random coincidence ABC, the complete operation is far from that of FIFO.

Finally, Examiner calls attention to Figure 8, t=t1, t=t4, and t=t5. However, a look at the entirety of Figure 8 also shows that the behavior shown in Figure 8 is also far from a FIFO.

t=t1 DISP A

t=t2 DISP A

t=t3 DISP A

t=t4 DISP B

t=t5 DISP C

t=t6 DISP A

It is well known in the art that in a FIFO, first-in-first-out is by rule. Thus, a structure that outputs in a variety of different orders, one of which by random chance, happens to be first-in-first-out is not a FIFO.

Accordingly, Appellant respectfully requests REVERSAL of the rejections to independent claims 1, 5, 8, and 11.

D. THE REJECTION TO CLAIM 16 SHOULD BE REVERSED

Claim 16 recites, among other limitations, "wherein the FIFO stores the indicators in a particular order, and wherein the display engine displays the images associated with the indicators in an order corresponding to the order that the indicators are stored in the FIFO".

Examiner has argued that "Adolph teaches the memory (16 of Fig 7) has FIFO opreation as described above and indicatores stored in the memories (A,B, and C of fig. 7) in a particular order (the memory A stores I0, col. 5, lines 23-24; the memory stores I1, col. 5, lines 24-25; the memory C stores B pictures, col. 5, lines 53-54; wherien DISP A for memory A, DISP B for memory [B}, DISP C for memory C; this would fairly suggest a particular order".

Appellant reiterates the remarks in section C, and respectfully submits that Adolph clearly doesn not teach "wherein the FIFO stores the indicators in a particular order, and wherein the display engine displays the images associated with the indicators in an order corresponding to the order that the indicators are stored in the FIFO". Accordingly, Assignee respectfully requests reversal of the rejection to claim 16.

VIII. CONCLUSION

For the foregoing reasons, claims 1-5, 7-14, 16-22, and 24-26 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: October 29, 2009

Respectfully submitted,

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CLAIMS APPENDIX

1. A system for displaying images on a display, said system comprising:

a decoder for decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;

image buffers for storing the decoded images;

a FIFO for storing indicators indicating images to be displayed; and

a display engine for presenting the images indicated by the FIFO for display.

2. The system of claim 1, further comprising:

parameter buffers for storing the decoded parameters associated with the images.

3. The system of claim 2, wherein the display engine presents the images indicated by the queue for display by receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

4. The system of claim 1, wherein the decoder comprises a first processor and the display engine comprises a second processor.

5. A method for displaying images on a display, said method comprising:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoded parameters associated with the decoded images;

storing the decoded images;

queuing indicators indicating images to be displayed in a FIFO; and

presenting the images indicated by a particular one of the indicators for display.

6. The method of claim 5, further comprising:

storing the decoded parameters associated with the images.

7. The method of claim 6, wherein presenting the images for display further comprises receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

8. A circuit for displaying images on a display, said circuit comprising:

a processor;

a memory operably coupled to the processor, said memory storing a plurality of executable instructions, wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;

storing the decoded images;

storing indicators indicating images to be displayed in a FIFO; and

presenting the images indicated by the stored indicators for display.

9. The circuit of claim 8, further comprising:

storing the decoded parameters associated with the images.

10. The circuit of claim 9, wherein the instructions causing presenting the images further comprise instructions causing receiving the decoded parameters and displaying the decoded images based on the decoded parameters.

11. A circuit for displaying images on a display, said circuit comprising:

a first processor;

a first memory operably coupled to the first processor, said first memory storing a plurality of instructions for execution by the first processor, wherein the plurality of executable instructions cause:

decoding encoded images and parameters associated with the images, thereby resulting in decoded images and decoder parameters associated with the decoded images;

storing the decoded images;

storing indicators indicating images to be displayed in a FIFO ; and

a second processor operably coupled to the queue;

a second memory operably coupled to the second processor, said second memory storing a plurality of instructions for execution by the second processor, wherein the plurality of executable instructions cause:

presenting the images indicated by the indicators for display.

12-15. (Cancelled)

16. The system of claim 1, wherein the FIFO stores the indicators in a particular order, and wherein the display engine displays the images associated with the indicators in an order corresponding to the order that the indicators are stored in the FIFO.

17. The system of claim 1, wherein each indicator indicates a different image to be displayed.

18. The method of claim 5, wherein each indicator indicates a different image to be displayed.

19. The circuit of claim 8, wherein each indicator indicates a different image to be displayed.

20. The circuit of claim 11, wherein each indicator indicates a different image to be displayed.

21. The circuit of claim 16, wherein the FIFO stores the indicators in the particular order prior to the display engine displaying the images associated with the indicators in the order corresponding to the order that the indicators are stored in the FIFO.

EVIDENCE APPENDIX

There are no pages in this appendix

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.